UNITED STATES PATENT AND TRADEMARK OFFICE

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09/519,282	03/07/2000	Daniel E Lenoski	97437	9726

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EXAMINER
MOORE, IAN N

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/519,282	LENOSKI ET AL.
	Examiner	Art Unit
	Ian N Moore	2661

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the amendment filed on 8-18-04*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7,9,10 and 26-28* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,9,10 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Independent claim 1 amended and new claims 26-28 are added.

2. Claims 2-5, 8,11-25 are cancelled.

Response to Arguments

3. Applicant's arguments with respect to claims 1,6,7,9,10 and 26-28 have been considered but

are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

4. Claim 7 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention.

Claim 7 recites the limitation "**a particular packet**" in line 3. It is unclear whether "**a**

particular packet" in line 3 and "**a particular packet**" claim 1 refers to the same packet.

Claim 26 recites, "…the particular packet, …one or more status data structure, includes

ANDing a plurality of bit vectors…" in line 4. It is unclear what is being ANDing with a

plurality of bit vectors. In particular, it is unclear whether ANDing is performed <u>between</u>

a) a plurality of bit vectors and one or more status data structure, or

b) a plurality of bit vectors and the particular packet, or

c) a plurality of bit vectors and the particular path.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi (U.S.

5,689,500) in view of Turner (U.S. 4,734,907).

Regarding claim 1, Chiussi'500 discloses a method preformed by a packet switch,

the packet witch including one or more multistage interconnection networks (see FIG. 11, a

first multistage interconnection network consists of input ASX 0-2, AXB 0-2 and output

ASX 0-2; and a second multistage interconnection network consists of input ASX 3-5, AXB

3-5 and output ASX 3-5), each of said one or more multistage interconnection networks

including a plurality of switching stages (see FIG. 11 input ASX 0-5, AXB 0-5 and output

ASX 0-5) which include a first switching stage (see FIG. 11, ASX 1133) and final switching

stage (see FIG. 11, ASX 1131), and one or more-intermediate switching stages in between

the first and final switching stages (see FIG. 11, AXB 1132), said or more intermediate

switching states including a broadcast component (see FIG. 11, backpressure processor 404

of AXB) the method comprising:

recognizing an error (see col. 13, lines 50-60; see col. 14, lines 21-26; the queue of

record counter exceeds current threshold) within the packet switch (see FIG. 1, ATM or

similar switch node; see col. 2, lines 26-32) by one of the plurality of switching stages (see

FIG. 11, one of the output ASX module 1133);

sending a particular packet (see FIG. 12, backpressure bitmap message) from said one

of the plurality of switching stages (see FIG. 11, one of the output ASX module 1133) to the

broadcast component (see FIG. 11, backpressure processor 404 of AXB 1132) through at

least a portion of said one or more interconnection network (see FIG. 11, a portion of one or

more multistage interconnection network which comprises input ASX 0-5, AXB 0-5 and

output ASX 0-5) in response to said recognizing the error (see col. 14, , lines 22-31; note that

upon detecting the threshold crossing, a backpressure bitmap message is send toward AXB

module 1132), the particular packet including an indication of the error (see FIG. 12, a

bitmap message indicates the switch backpressure bit map); and

notifying a plurality of input component if the packet switch of the error (see FIG. 11,

sending backpressure bitmap message to input/ingress side of the port cards 1110; see col.

14, lines 44-47), said notifying including sending one or more packets indicating the error

from the broadcast component (see FIG. 1, a backpressure bitmap message is sent from

backpressure processor 404 of AXB 1132 to ASX modules) through at least a second portion

of said one or more interconnection networks (see FIG. 11, a portion of one or more

multistage interconnection network which comprises input ASX 0-5 and AXB 0-5), said

second portion including the final switching state (see FIG. 11, input ASX 1131; see col. 14,

line 35-50).

Chiussi'500 does not explicitly disclose an indication corresponding to the broadcast

component.

However, the above-mentioned claimed limitations are taught by Turner'907. In

particular, Turner'907 teaches the particular packet including an indication corresponding to

the broadcast component (see FIG. 4, BCN, broadcast control channel, and LCN, logical

control channel; see FIG. 13A, a broadcast packet contains indication B for broadcasting, and

indication BCN which corresponds to broadcast node (i.e. 362); see col. 4, lines 35, lines 35

to col. 5, lines 25; see col. 14, lines 20-45).

However, this limitation is taught by Turner'907. It would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify the system of

Sheu'227, as taught by Turner'907 for the purpose of broadcasting a packet with broadcast

indication over the stages of network within a switch since Turner'907 states at col. 1, lines

that it will provide a high performance packet switch which is capable of efficient operation

in broadcast mode. The motivation being that by broadcasting the packet via the stages

within the switch with BCN and B indication, it can reduce the processing time/cost of a

single node/component broadcasting to every node/component since the processing/load will

be distribute to the secondary node/component will broadcast the rest of the network; thus

increasing the performance of the packet switch. Moreover, by utilizing indication B and

BCN, the system can easily identified the type of packet; see col. 4, lines 20-30.

6. Claims 6,7,9, 10, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chiussi'500 and Turner'907, as applied to claim 1 above, and further in view of Soloway

(U.S. 5,265,092).

Regarding Claim 6, Chiussi'500 discloses the input component updating in response to receiving a notification of the error (see col. 10, lines 1-5, col. 14, lines 44-51; col. 15, lines 1-27; note that upon receiving backpressure bitmap message at the ingress side of the port card, the input port card performs updating by stop sending the cells to that specified congested route and port).

Chiussi'500 does not explicitly disclose each component (see Soloway'092 FIG. 1, Switches 4a-4d) updating one or more status data structures (see Soloway'092 FIG. 2, Forwarding Table) in response to receiving a notification of the error (see Soloway'092 col. 3, line 1-23; note that LSP packet is send to each switch in the network in order to broadcast/notify the congested/failure/affected/error in the link. Upon receiving LSP packet, each switch updates the forwarding table accordingly).

However, this limitation is taught by Soloway'092. Note that Chiussi'500 teaches receiving a backpressure bitmap message/packet at each ingress side of the port module regarding the congested stages, and the each ingress side of the port performs updates by stop sending to that specified congested link. Soloway'092 teaches receiving LSP packets which indicates the links that are affected by the congestion/error at each switch in the network, and each switch update the routing accordingly by stop forwarding/routing to the specified affected link. Soloway'092's packet routing/switching technique/functionality can be used to modify Chiussi'500's switch. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Chiussi'500 and Turner'907, as taught by Soloway'092 for the purpose of receiving LSP packet and update the routing table at each switch accordingly, since Soloway'092 states in col. 3, lines 1-24 that it

will achieve loop-free routing of data packets. The motivation being that by updating the

forwarding table in each switch upon receiving an LSP packet, it can readily switchover to

available/configured route/path/link, which increase the routing efficiency and reduce the

routing loop.

Regarding claim 7, the combined system of Chiussi'500, Turner'907, and

Soloway'092 teaches each of the plurality of input components (see Chiussi'500 FIG. 11,

Ingress side of port cards 0-17), a plurality of paths (see Turner'907 FIG. 11, links 1120,

1134, 1140) leading to a destination output component (see Chiussi'500 FIG. 11, Egress side

of port cards 0-17) over which to send a particular packet (see Chiussi'500 FIG. 11,

backpressure bitmaps message), and the data structure (see Soloway'092 FIG. 2, Forwarding

table) as described above in Claim 6.

Soloway'092 discloses each of the plurality of components determining which of a

plurality of paths leading to a destination component over which to send a particular packet,

the path determined by referencing the one or more status data structures (see FIG. 2,

forwarding table, and FIG. 4, Forwarding Process logic 40, Forwarding Table 36, Routing

Logic 38, LSP Database; col. 3, line 15-5; note that the each switch re-computes/determines

each route to the destination switch/end-node according to shortest path routing algorithm.

Then after, the packets are routed according to the switchover or reconfigured paths/links

toward the destination).

Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to modify the combined system of Chiussi'500 and Turner'907,

as taught by Soloway'092 by providing a mechanism to recomputed/re-calculate/determines

the shortest paths/routes toward the destination in the forwarding table for the same reason

stated in Claim 6 above.

Regarding claim 9, the combined system of Chiussi'500, Turner'907, and

Soloway'092 teaches each of the plurality of input components (see Chiussi'500 FIG. 11,

Ingress side of port cards 0-17), a plurality of paths (see Turner'907 FIG. 11, links 1120,

1134, 1140) leading to a destination output component (see Chiussi'500 FIG. 11, Egress side

of port cards 0-17) over which to send a particular packet (see Chiussi'500 FIG. 11,

backpressure bitmaps message), and the data structure (see Soloway'092 FIG. 2, Forwarding

table) as described above in Claim 6.

Soloway'092 discloses wherein the one or more data structures include an output

availability table to indicate whether a possible path through the packet switching system

from the input component to a particular destination is available (see FIG. 2, forwarding table

with hold down bit for channel 8a at switch 4d see col. 8, lines 12-61; note that when LSP

packet indicates that channel 8a is the affected channel/link, the forwarding table is updated

with hold-down bit as an entry for that particular channel/link. Thus, the channels/links

toward the destinations, which are not indicated by the hold-down bit, are the

available/candidate paths/links.)

Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to modify the combined system of Chiussi'500 and Turner'907

as taught by Soloway'092 by providing a mechanism to indicate the affected channel/link

toward the destination in order to determine/identify the available/candidate links for the

same reason stated in Claim 6 above.

Regarding Claim 10, Chiussi'500 discloses disabling at least one of the plurality of

input components from sending packets to a particular destination of the packet switching

system when a path in the packet switching system leading to a particular destination falls

below a predetermined threshold value as identified by one or more received packets

containing indications of one more error (see col. 10, lines 1-5, col. 14, lines 44-51; col. 15,

lines 1-27; note that the ingress side of the port card stops sending the cells to that particular

congested route and output port of the packet switch after receiving backpressure bitmap

message. A backpressure bitmap message is generated when the system detects that the

acceptable threshold for cell transmission is exceeded in the path towards the destination; see

col. 13, lines 49-67. As stated above 1 claim 1, a backpressure bitmap message contains

congestion indication/error).

Chiussi'500 does not explicitly disclose a number of possible paths in the packet

switching system leading to a particular destination.

However, this limitation is taught by Soloway'092. In particular, Soloway'092

disclose disabling at least one of the plurality components (see Soloway'092 FIG. 1, Switches

4a-4d) from sending packets to a particular destination through the packet switching system

leading to a particular destination as identified by one or more received packets containing

indications of one or more errors (see Soloway'092 FIG. 2, forwarding table with hold down

bit for channel 8a at switch 4d; col. 8, lines 12-61; col. 3, line 1-23; note that LSP packet is

send to each switch in the network in order to broadcast and notify the link state. Upon

receiving LSP packet, each switch updates the forwarding table accordingly. In particular,

when the LSP packet indicates that channel 8a is the affected channel/link, the forwarding

table is updated with hold-down bit as an entry for that particular channel/link. Thus, the

channels/links toward the destinations, which are indicated by the hold-down bit, are the

disable switches/links/paths).

Note that Chiussi'500 teaches receiving a backpressure bitmap message/packet at

each ingress side of the port module regarding the congested stages, and the each ingress side

of the port performs updates by stop sending to that specified congested link. Soloway'092

teaches receiving LSP packets, which indicates the links that are affected by the

congestion/error at each switch in the network, and each switch, update the routing

accordingly by stop forwarding/routing to the specified affected link. Soloway'092's packet

routing/switching technique/functionality can be used to modify Chiussi'500's switch. It

would have been obvious to one having ordinary skill in the art at the time the invention was

made to modify the combined system of Chiussi'500 and Turner'907, as taught by

Soloway'092 by providing a mechanism to indicate the affected/disable channel/link toward

the destination for the same reason stated in Claim 6 above.

Regarding Claim 27, Chiussi'500 discloses wherein the predetermined threshold

value is greater than one (see col. 13, lines 49-67; note that the acceptable/threshold queue

size must be greater than one, since the queue is cell transmission queue in the ATM switch.

The ATM switch queue is capable of handling more that one cell).

Regarding Claim 28, Chiussi'500 discloses disabling at least one of the plurality of

input components from sending packets to a particular destination of the packet switching

system when a path in the packet switching system leading to a particular destination falls

below a predetermined threshold value (see col. 10, lines 1-5, col. 14, lines 44-51; col. 15,

lines 1-27; note that the ingress side of the port card stops sending the cells to that particular

congested route and output port of the packet switch after receiving backpressure bitmap

message. A backpressure bitmap message is generated when the system detects that the

acceptable threshold for cell transmission is exceeded in the path towards the destination; see

col. 13, lines 49-67).

Chiussi'500 does not explicitly disclose a number of possible paths in the packet

switching system leading to a particular destination.

However, this limitation is taught by Soloway'092. In particular, Soloway'092

disclose disabling at least one of the plurality components (see Soloway'092 FIG. 1, Switches

4a-4d) from sending packets to a particular destination through the packet switching system

leading to a particular destination as identified by one or more received packets containing

indications of one or more errors (see Soloway'092 FIG. 2, forwarding table with hold down

bit for channel 8a at switch 4d; col. 8, lines 12-61; col. 3, line 1-23; note that LSP packet is

send to each switch in the network in order to broadcast and notify the link state. Upon

receiving LSP packet, each switch updates the forwarding table accordingly. In particular,

when the LSP packet indicates that channel 8a is the affected channel/link, the forwarding

table is updated with hold-down bit as an entry for that particular channel/link. Thus, the

channels/links toward the destinations, which are indicated by the hold-down bit, are the disable switches/links/paths).

Note that Chiussi'500 teaches receiving a backpressure bitmap message/packet at each ingress side of the port module regarding the congested stages, and the each ingress side of the port performs updates by stop sending to that specified congested link. Soloway'092 teaches receiving LSP packets which indicates the links that are affected by the congestion/error at each switch in the network, and each switch update the routing accordingly by stop forwarding/routing to the specified affected link. Soloway'092's packet routing/switching technique/functionality can be used to modify Chiussi'500's switch. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Chiussi'500 and Turner'907, as taught by Soloway'092 by providing a mechanism to indicate the affected/disable channel/link toward the destination for the same reason stated in Claim 6 above.

Neither Chiussi'500, Turner'907, nor Soloway'092 explicitly discloses the number of possible path/threshold equal 1. Chiussi'500 teaches acceptable threshold of one or more cell in each queue for each link and stopping the cell transmission upon receiving backpressure message. Soloway'092 teaches having a forwarding table, which lists the affected links and non-affected links due to link error, and stopping the transmission towards the affected link. Setting the number of possible path/threshold to 1 does not define a patentable distinct invention over that in the combined system of Chiussi'500, Turner'907 and Soloway'092 since both the invention as a whole and the combined system of Chiussi'500, Turner'907and Soloway'092 are directed to determining whether to stop or start sending cells/packets upon

error/backpressure message and stopping when the threshold is exceed or when the threshold

exceeding message is received, so as to maintain the packet/cell transmission reliability and

avoiding packet/cell lost in the network by controlling the congestion and other link error.

The degree in which determining threshold value presents no new or unexpected results, so

long as the packet/cell transmission is maintained and no packet/cell are lost, and the

packet/cell is processed and transmitted in a successful way. If one has less number of link

thresholds to determine when to stop transmission, it will be provide excellent or good

service which can be used for more delay/error sensitive cell/packet, and if one has more

number of link thresholds, it will provide fair service which can be used for lesser delay/error

sensitive cell/packet. Therefore, to have threshold path of 1, that to maintain the packet/cell

transmission reliability and to avoid packet/cell lost in the network by controlling the

congestion and other link error, would have been routine experimentation and optimization in

the absence of criticality.

Allowable Subject Matter

7. Claim 26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112,

2nd paragraph, set forth in this Office action and to include all of the limitations of the base

claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The

examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ken Vanderpuye can be reached on 571-272-3078. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
10/1/04

BRIAN NGUYEN
PRIMARY EXAMINER